## **LAB 1**

## OBJECTIVE: To design and simulate a 2-input AND gate using VHDL, and verify its functionality using a testbench.

## TOOLS USED:

* VHDL (VHSIC Hardware Description Language)
* <https://www.edaplayground.com/> (for simulation)

**THEORY:**

The aim of this lab is to create a simple 2-input AND gate in VHDL and simulate it using a testbench. The design code describes the logic of the AND gate, and the testbench applies all possible input combinations to validate the behavior of the gate.

## VHDL CODE

**DESIGN:**

library ieee;

use ieee.std\_logic\_1164.all;

entity andgate is

port( a,b:in std\_logic;

c: out std\_logic);

end andgate;

architecture behavior of andgate is

begin

c <= a and b;

end behavior;

**TESTBENCH**

library ieee;

use ieee.std\_logic\_1164.all;

entity andgate\_tb is

---> no content

end andgate\_tb;

architecture test of andgate\_tb is

component andgate

port(a,b: in std\_logic;

c: out std\_logic);

end component;

signal ak,bk,ck: std\_logic;

begin

and\_gate: andgate port map(a=>ak, b=>bk, c=>ck);

process begin

ak <= '0';bk <= '0';wait for 1 ns;

ak <= '0';bk <= '1';wait for 1 ns;

ak <= '1';bk <= '0';wait for 1 ns;

ak <= '1';bk <= '1';wait for 1 ns;

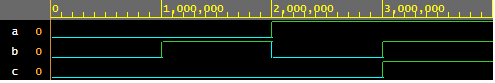
assert false report "Completed successfully";

wait;

end process;

end test;

Output:



CONCLUSION:

The 2-input AND gate was successfully simulated. The output matched the expected truth table for all input combinations. The use of a simple testbench allowed for effective verification of the circuit behavior in a VHDL simulation environment.